**ECE -1 Lab **

**Experiment - 2**

Aim: Realize the function, mentioned below in at least four different physical ways:

F(x) = x0 + x1 + x2 + x3 + x4 + x5 + x6 + x7 + x8 + x9

Description:

Part 1:

1. Implement the Function F(x) using 8 stages of 2 input OR gates in schematic design environment.
2. Implement F(x) using three 4 different input OR gates. ( 3 gates each having 4 inputs)
3. Implement F(x) as a three stage network. (Longest path should have 3 gates and any gate can have any number of inputs)
4. Implement F(x) as a 4 stage network.

Part 2:

1. Select any Spartan-III and CPLD device.
2. Generate the synthesis report and analyze the resources used (for e.g. gates, slices, IOB etc.), as well as the combinational path delay.
3. Compare the delay, power and cell usage in all 4 different implementation.